AMENDMENTS TO THE CLAIMS

Claims 1-9. (canceled)

Claim 10. (new) A channel decoder for a digital broadcast receiver, comprising:

a synchronization byte detector for detecting synchronization bytes in a decoded transmission signal;

wherein said synchronization byte detector provides a synchronization signal indicating a start of frame for transport stream packets in the decoded transmission signal; and

wherein the synchronization byte detector provides a lock detected output signal indicating the receiver is locked-in to one broadcast channel;

said lock detected output signal being used as at least one of a feed forward signal and a feed back signal to switch processing stages at least one of succeeding and preceding, respectively, said synchronization byte detector into a different mode dependent on whether or not a lock has been achieved.

Claim 11. (new) The channel decoder according to claim 10, wherein at least one of a clock and a carrier recovery circuit preceding the synchronization byte detector is switched from a robust mode used for acquisition of a broadcast channel to a locked mode used for compensation of small deviations of an acquired broadcast channel when the receiver is locked-in and vice-versa when the receiver is not locked-in.

Claim 12. (new) The channel decoder according to claim 10, wherein the loop bandwidth of at least one of a clock and a carrier recovery loop within the clock and carrier

recovery circuit is switched from a wide bandwidth mode that allows a fast coarse lock of the receiver to the clock and a carrier of a transmission signal to a narrow bandwidth mode, respectively, which performs a low noise fine adjustment of the receiver to the clock and the carrier of the transmission signal, respectively, when the receiver is locked-in and vice-versa when the receiver is not locked-in.

Claim 13. (new) The channel decoder according to claim 10, wherein an adaptive equalizer within the channel decoder is switched from an acquisition mode to a tracking mode when the receiver is locked-in and vice-versa when the receiver is not locked-in.

Claim 14. (new) The channel decoder according to claim 10, further comprising:

a forward error correction stage succeeding the synchronization byte detector;

said forward error correction stage being switched from an off mode to an on mode when the lock detected output signal indicates the receiver is locked-in; and

said forward error correction stage being switched from the on mode to the off mode when the lock detected output signal indicates the receiver is not locked-in.

Claim 15. (new) The channel decoder according to claim 14, wherein all stages succeeding the forward error correction stage are switched from an off mode to an on mode when the receiver is locked-in and vice-versa when the receiver is not locked-in.

Claim 16. (new) The channel decoder according to claim 10, further comprising an output port to output said lock detected output signal to other processing stages within the

receiver.

Claim 17. (new) The channel decoder according to claim 10, wherein the channel decoder is used in a digital video broadcasting receiver or in a digital audio broadcasting receiver.

Claim 18. (new) The channel decoder according to claim 10, wherein the channel decoder is used for satellite, cable or terrestrial reception.